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IN THE
UNITED STATES
PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	Denison et al.
CASE:	MET-041424C004
SERIAL NO.:	10/807,936
FILING DATE:	March 24, 2004
FOR:	ELECTRONIC ACCESS CONTROL DEVICE

COMMUNICATION

Box Amendment
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION OF:
Art Unit 2635
EXAMINER:
Nguyen, Nam V.

Dear Examiner Nguyen:

Per MPEP § 713.04, this is a summary of the telephone interview that took place on May 23, 2009 between the Examiner and Applicant and Applicant's counsel.

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SUMMARY

Applicant thanks the Examiner for the professional courtesies extended in a telephone interview held on May 22, 2009 with Applicant (inventor William D. Denison) and Applicant's counsel (Joseph M. Kinsella Jr.) wherein new Claims 201-210 were discussed with the Examiner.

Per the Examiner's request, Applicant herein provides citations showing support for Claims 201-210.

In particular, independent Claim 201 and dependent claims 202, 204, 205, 206, 207, 208—which are related to Claims 1, 5, 16, 23, and 27 of Applicant's U.S. Patent No. 7,295,100—includes, among other things:

(1) a memory comprising a time and/or date value;
(2) a communication port configured to communicate:
  i) a serial number;
  ii) the input code; and,
  iii) the time and/or date value while the first processor is in an activated mode.
(3) a memory having stored therein at least one access code and a serial number;
(4) a first and a second processor;
(5) a first and second state electromechanical driver; and,
(6) a low voltage detection circuit.

In the specification as filed, the "time and/or date value" and the "serial number" stored in a memory are disclosed at page 14, lines 20-25.

The "communication port configured to communicate . . . while the first processor is in an activated mode" is disclosed at page 13, line 5 to page 14, line 15.

Figure 4 discloses the processor being in an activated mode while beginning communication, and entering a sleep mode when finished.

The first and second processor arrangement is shown in Figure 9 and disclosed at page 24, line 16 to page 27, line 16.

The first and second state electromechanical drivers and timer are disclosed at page 16, line 25 to page 17, line 31.

The low voltage detection circuit is disclosed at page 23, line 10 to page 24, line 15.

With regard to Claims 203 and 209, support for Claim 203 is disclosed at page 32, line 3 to page 33, line 8; and, support for Claim 209 is disclosed at page 26, lines 4-15.

In view of the above, Applicant submits that all pending claims are patentably distinct over the cited prior art references and fully supported by the specification. As such, Applicant respectfully requests that the objections and rejections be removed and all pending claims be allowed to issue.

Should the Examiner have any questions or comments regarding the above, a telephone call to the undersigned at (312) 226-1818 is respectfully requested.

Respectfully submitted,

Dated: May 26, 2009

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CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope Addressed to: Mail Stop-Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 26, 2009
Yolanda Solis